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Date: April 7, 1997

Attached for filing is the patent application of:

Inventor: TANAKA et al

Entitled: LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF DRIVING THE SAME

and including attachments as noted below:

- [ X ] Declaration, [ X ] Abstract  
[ 41 ] pages of specification and claims (including 17 numbered claims), and  
[ 8 ] sheets of accompanying drawing/s.  
[ X ] Record & return the attached assignment to the undersigned.  
[ X ] Priority is hereby claimed under 35 USC 119 based on the following foreign applications:

Application Number	Country	Day/Month/Year Filed
8-100073	Japan	22 April 1996

, respectively.

Certified copy(ies) of foreign application(s): [ X ] attached; [ ] filed on \_\_\_\_\_  
in U.S. Application Serial No. \_\_\_\_\_ filed on \_\_\_\_\_  
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- [ ] Please amend the specification by inserting before the first line -- This is a of PCT application ,  
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- [ ] Verified Statement attached establishing "small entity" status (Rules 9 & 27).  
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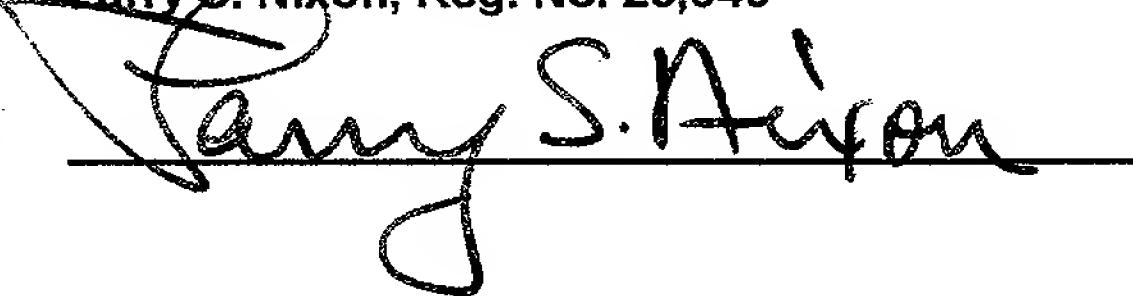
Basic filing fee .....	\$ 770.00
Total effective claims 17 - 20 (at least 20) = 0 x \$22 .....	\$ 0.00
Independent claims 2 - 3 (at least 3) = 0 x \$80 .....	\$ 0.00
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SUBTOTAL .....	\$ 770.00
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SECOND SUBTOTAL .....	\$ 770.00
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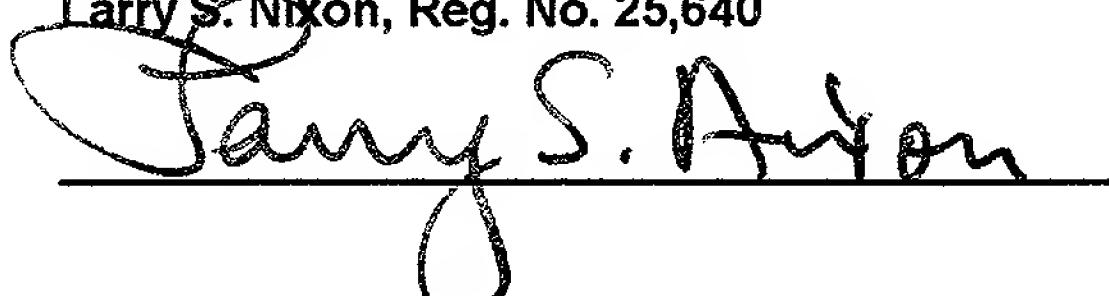
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# ***U.S. PATENT APPLICATION***

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Takayuki Shimada  
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Mikio Katayama*

***Invention:*** *LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF  
DRIVING THE SAME*

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## ***SPECIFICATION***

- 1 -

## LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF DRIVING THE SAME

### FIELD OF THE INVENTION

The present invention relates to an active matrix type liquid crystal display device having switching elements, such as thin film transistors, arranged in a matrix pattern, and a method of driving the liquid crystal display device.

### BACKGROUND OF THE INVENTION

The following description will discuss an active matrix type liquid crystal display device.

For example, as illustrated in Fig. 10, the liquid crystal display device is constructed by sealing liquid crystals 2 in the space between a pair of upper and lower transparent glass substrates 1b and

1a.

As shown in Fig. 9, formed on the lower substrate 1a are scanning lines  $3_1$ ,  $3_2$  ..., and signal lines  $4_1$ ,  $4_2$  ... intersecting the scanning lines  $3_1$ ,  $3_2$  ... at right angles. The scanning lines  $3_1$ ,  $3_2$  ... are formed by a conducting film, and scanning signals from a scanning drive circuit K are successively applied to the scanning lines  $3_1$ ,  $3_2$  .... On the other hand, the signal lines  $4_1$ ,  $4_2$  ... are formed by a conducting film, and data signals from a data drive circuit L are successively applied to the signal lines  $4_1$ ,  $4_2$  ....

Mounted in the vicinity of each of the intersections of the scanning lines  $3_1$ ,  $3_2$  ... and the signal lines  $4_1$ ,  $4_2$  ... are a thin film transistor (TFT) 5 as a switching element, and a pixel electrode 6 formed by a conducting film. The TFT 5 is electrically connected to both of the lines, and the pixel electrode 6 is connected to the TFT 5.

As shown in Fig. 10, a common electrode 7 and a color filter 8 are mounted on the upper glass substrate 1b. The common electrode 7 is formed by a transparent conducting film and connected to a common line 9 to which a common signal is applied. The pixel electrode 6 and the common electrode 7 form a capacitor 12 for ensuring a liquid crystal capacitance

$C_{LC}$  as shown in Fig. 11.

As illustrated in Fig. 9, in the TFT 5, a gate electrode 5g is connected to each of the scanning lines  $3_1$ ,  $3_2$  ..., a source electrode 5s is connected to each of the signal lines  $4_1$ ,  $4_2$  ..., and a drain electrode 5d is connected to the pixel electrode 6.

Moreover, an additional capacitance line 10 formed by a conducting film is arranged below the pixel electrode 6, and connected to the common line 9. Considering an improvement of the data retentivity of the liquid crystals 2 to achieve high image quality, a capacitor 13 for ensuring an additional capacitance  $C_s$  is formed by the pixel electrode 6 and the additional capacitance line 10 as shown in Fig. 11.

In the liquid crystal display device of the above-mentioned structure, for example, when scanning signals are successively input downward from the scanning drive circuit K to the scanning lines  $3_1$ ,  $3_2$  ..., the gates of a line of the TFTs 5 are simultaneously turned ON by the input of the scanning signals, and a display-use data signal is input for each pixel from the signal lines  $4_1$ ,  $4_2$  ... by the data drive circuit L. As a result, the data signal is applied to the pixel electrode 6, and the transmittance of the liquid crystals 2 is changed by

the potential difference between the pixel electrode 6 and the common electrode 7.

In this case, when a direct current continues to be supplied over a long time, the data retentivity of the liquid crystals 2 deteriorate. Therefore, the liquid crystals 2 are driven by a so-called AC drive method in which a positive voltage and a negative voltage are alternately applied to the pixel electrode 6 by switching the polarity of data signals to be input to the signal lines  $4_1, 4_2 \dots$ , for example, every horizontal period.

As the ideal capacitance (pixel capacitance) for a single pixel, in general, only the liquid crystal capacitance  $C_{LC}$  and the additional capacitance  $C_s$  exist between the pixel electrode 6 and the common electrode 7 and between the pixel electrode 6 and the additional capacitance line 10, respectively, as shown in Fig. 11.

Actually, when conducting films are placed parallel to each other or conducting films are placed one upon another with an insulating film therebetween, a parasitic capacitance is generated between the conducting films. For example, as shown in Fig. 15, in a pixel located in the second row and the first column, i.e., a pixel in which the gate of the TFT 5

is connected to the second scanning line from the top,  $3_2$ , and the source thereof is connected to the first signal line from the left,  $4_1$ , the periphery of the pixel electrode 6 is enclosed by the upper and lower scanning lines  $3_1$  and  $3_2$ , and the right and left signal lines  $4_1$  and  $4_2$  as shown in Fig. 9. Therefore, as illustrated in Fig. 12, parasitic capacitances  $C_{gd_2}$ ,  $C_{gd_1}$ ,  $C_{sd_2}$  and  $C_{sd_1}$  are generated between the pixel electrode 6 and the lines  $3_1$ ,  $3_2$ ,  $4_1$ ,  $4_2$ , respectively.

The parasitic capacitance ratio in this pixel is given by

$$\alpha = \Delta C / (C_{LC} + C_s + \Delta C) \quad \dots \dots \quad (1)$$

where  $\Delta C = C_{gd_1} + C_{gd_2}$ .

When driving the liquid crystals 2 by the above-mentioned AC drive method, such a parasitic capacitance ratio  $\alpha$  affects the fluctuation  $\Delta V$  of a voltage applied to the pixel electrode 6, and the voltage fluctuation  $\Delta V$  generates a DC component, resulting in deterioration of the data retentivity. In order to prevent the generation of the DC component, in prior arts, optimization is performed for each gray scale according to the parasitic capacitance ratio  $\alpha$ .

The above explanation of the parasitic capacitance generated in each pixel is given for a

pixel whose TFT 5 is connected to the scanning line  $3_2$ , located in the second row from the top.

Next, with reference to a pixel whose TFT 5 is connected to the topmost scanning line  $3_1$  from which the scanning of scanning signal is initiated, the following description will explain a parasitic capacitance generated in this pixel. Since any scanning line is not present above the pixel electrode 6 constituting this pixel, the parasitic capacitance  $C_{gd_2}$  is not generated.

Therefore, in this case, the parasitic capacitance ratio is given by

$$\alpha' = \Delta C' / (C_{Lc} + C_s + \Delta C') \quad \dots \dots \quad (2)$$

where  $\Delta C' = C_{gd_1}$ .

Namely, the parasitic capacitance ratio in the pixels corresponding to the scanning lines  $3_2, 3_3 \dots$  other than topmost scanning line  $3_1$  becomes the parasitic capacitance ratio  $\alpha$  given by Equation (1) because these scanning lines are all symmetrically arranged about the additional capacitance line 10 as shown in Fig. 9. However, since the topmost scanning line  $3_1$  is not symmetrical about the additional capacitance line 10, the parasitic capacitance ratio in the pixels corresponding to the topmost scanning lines  $3_1$  becomes the parasitic capacitance  $\alpha'$  given by

Equation (2).

Thus, the parasitic capacitance ratio in the pixels corresponding to the topmost scanning line  $3_1$  differs from the parasitic capacitance ratio in the pixels corresponding to the scanning lines  $3_2$ ,  $3_3$  ... located after the first row.

As described above, optimization is performed for the pixels corresponding to the scanning lines  $3_2$ ,  $3_3$  ... after the first row so as to reduce the influence of the parasitic capacitance ratio  $\alpha$  and prevent the application of a DC component to the liquid crystals 2.

However, since the parasitic capacitance ratio  $\alpha'$  in the pixels corresponding to the topmost scanning line  $3_1$  differs from the parasitic capacitance ratio in the pixels corresponding to other scanning lines, the fluctuation  $\Delta V$  of the voltage to be applied to the pixel electrodes 6 cannot be eliminated. As a result, an extremely small DC component is applied to the liquid crystals 2 in the pixels corresponding to the first scanning line  $3_1$ , and therefore the data retentivity of the liquid crystals 2 deteriorate with time.

Consequently, a line of pixels corresponding to the topmost scanning lines  $3_1$  may cause a defect, for

example, a bright line, deteriorating the display quality. In this case, for example, if the liquid crystals 2 are of normally white type, a bright line appears in the halftone display. On the other hand, if the liquid crystals 2 are of normally black type, a black line appears in the halftone display. Such a phenomenon is particularly noticeable when a current is supplied under high temperatures.

#### SUMMARY OF THE INVENTION

It is an object of the present invention to provide a liquid crystal display device and a drive method thereof, capable of preventing defects such as the deterioration of display quality due to the appearance of particular pixels as a bright line by ensuring an equal parasitic capacitance for pixels of any locations.

In order to achieve the above object, a liquid crystal display device of the present invention includes:

a pair of substrates sandwiching liquid crystals therebetween;

a plurality of scanning lines to which scanning signals are successively applied;

a plurality of signal lines to which data signals

are successively applied, the signal lines intersecting the scanning lines at right angles;

a switching element which is arranged in the vicinity of each of the intersections of the scanning lines and the signal lines, and electrically connected to both of the scanning and signal lines;

a pixel electrode connected to each of the switching elements;

the scanning lines, signal lines, switching elements and pixel electrodes being formed on one of the substrates,

a common electrode formed on the other of the substrates so that the common electrode faces the pixel electrode with the liquid crystals therebetween;

a common line for supplying a common signal to the common electrode;

a pixel capacitance, one of electrodes of the pixel capacitance formed by the pixel electrode being connected to the common line; and

a dummy scanning line formed outside of one of the scanning lines located at an outermost position on either a scanning start side or a scanning end side of scanning signal.

In this liquid crystal display device, an equal parasitic capacitance is formed in any pixels

irrespectively of their positions by providing the dummy scanning line. This structure reduces conventional defects caused by unequal parasitic capacitances in the respective pixels, i.e., defects such as the deterioration of display quality due to the appearance of particular pixels as a bright line.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing the structure of a liquid crystal display device according to Embodiment 1 of the present invention.

Fig. 2 is a timing chart for inputting signals to a dummy scanning line and scanning lines in the liquid crystal display device shown in Fig. 1.

Fig. 3 is a circuit diagram showing the structure of a liquid crystal display device according to Embodiment 2 of the present invention.

Fig. 4 is a timing chart for inputting signals to a dummy scanning line and scanning lines in the liquid crystal display device shown in Fig. 3.

Fig. 5 is a circuit diagram showing the structure

of a liquid crystal display device according to Embodiment 3 of the present invention.

Fig. 6 is a timing chart for inputting common signals to a dummy scanning line in the liquid crystal display device shown in Fig. 5.

Fig. 7 is a timing chart for inputting signals to a dummy scanning line in the liquid crystal display device shown in Fig. 1 according to another example.

Fig. 8 is a graph showing results of examination of the occurrence of a blanking line in the respective embodiments.

Fig. 9 is a plane view showing the structure of a single pixel on a display panel of an active matrix type liquid crystal display device.

Fig. 10 is a cross sectional view of Fig. 9 cut across the A-A' line.

Fig. 11 is a diagram of an equivalent circuit of a capacitance which is generated in an ideal state in the single pixel shown in Fig. 9.

Fig. 12 is a diagram of an equivalent circuit of a capacitance which is generated in an actual state in the single pixel shown in Fig. 9.

Fig. 13 is a plane view of a single pixel of a liquid crystal display device according to Embodiment 6 of the present invention.

Fig. 14 is a cross sectional view of Fig. 13 cut across the B-B' line.

Fig. 15 is a circuit diagram showing the structure of a conventional liquid crystal display device.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

##### [Embodiment 1]

The following description will discuss one embodiment of the present invention.

In this embodiment, an active matrix type liquid crystal display device will be explained as a liquid crystal display device. The display mode of the liquid crystal display device is a super video graphics array (SVGA) mode. The same can be said for embodiments discussed later.

As illustrated in Fig. 1, the liquid crystal display device includes scanning lines  $3_1, 3_2, \dots$ , and signal lines  $4_1, 4_2, \dots$  intersecting the scanning lines  $3_1, 3_2, \dots$  at right angles. The scanning lines  $3_1, 3_2, \dots$  are formed by a conducting film. Scanning signals from a scanning signal drive circuit K are successively applied to the scanning lines  $3_1, 3_2, \dots$ . On the other hand, the signal lines  $4_1, 4_2, \dots$  are formed by a conducting film. Data signals from a data

drive circuit L are successively applied to the signal lines  $4_1, 4_2, \dots$

Disposed in the vicinity of the intersections of the scanning lines  $3_1, 3_2, \dots$  and signal lines  $4_1, 4_2, \dots$  are thin film transistors (TFTs) 5 as switching elements which are electrically connected to both of the lines, and pixel electrodes 6 which are formed by a conducting film and connected to the TFTs 5.

A dummy scanning line  $3_0$  for producing a capacitance is arranged outside of the scanning lines  $3_1, 3_2, \dots$ , i.e., outside of the outermost scanning line  $3_1$  arranged at a scanning start position from which the scanning of scanning signal starts. The dummy scanning line  $3_0$  is parallel to and faces the scanning line  $3_1$  with the pixel electrode 6 connected to the TFT 5 connected to the scanning line  $3_1$  therebetween.

More specifically, the dummy scanning line  $3_0$  is arranged at the same pitch as the pitch of other adjacent scanning lines, for example,  $3_1$  and  $3_2$ , so that the pixel electrode 6 is located between the dummy scanning line  $3_0$  and the scanning line  $3_1$ . The dummy scanning line  $3_0$  will be explained in detail later.

The pixel electrode 6 is formed by a transparent

conducting film, aluminum, etc. For example, as illustrated in Fig. 9, an additional capacitance line 10 formed by a conducting film is arranged below the pixel electrode 6. A common line 9 is connected to the additional capacitance line 10. Fig. 10 is a cross sectional view showing the vicinity of the junction of the pixel electrode 6 and the TFT 5.

As illustrated in Fig. 10, the above-mentioned liquid crystal display device is constructed by sealing in liquid crystals 2 between a pair of upper and lower transparent glass substrates 1b and 1a.

Formed on the lower glass substrate 1a are a gate electrode 5g of the TFT 5, and a gate insulating film 20 covering the gate electrode 5g.

An i layer 22 and an n<sup>+</sup> layer 23 are successively formed by amorphous Si on the gate insulating film 20 at the position corresponding to the gate electrode 5g. Formed on the n<sup>+</sup> layer 23 of amorphous Si are a source electrode 5s and a drain electrode 5d of the TFT 5. The pixel electrode 6 is formed in a pixel region on the gate insulating film 20. The pixel electrode 6 is connected to the drain electrode 5d.

Namely, in the TFTs 5, the gate electrodes 5g are connected to the scanning lines 3<sub>1</sub>, 3<sub>2</sub>, ..., the source electrodes 5s are connected to the signal liens 4<sub>1</sub>, 4<sub>2</sub>,

..., and the drain electrodes 5d are connected to the pixel electrodes 6.

On the other hand, a color filter 8 and a common electrode 7 are successively formed on the upper glass substrate 1b. The common line 9 (Fig. 1) to which a common signal is applied is connected to the common electrode 7. The color filter 8 is made of three primary colors, red, green and blue, and placed in a position corresponding to each pixel electrode 6.

An alignment film (not shown) for aligning the liquid crystals 2 is formed to cover the pixel electrode 6. Similarly, on the upper glass substrate 1b, an alignment film (not shown) is formed to cover the common electrode 7.

Further, a polarizing plate (not shown) is mounted on outer surfaces of the glass substrates 1a and 1b, i.e., surfaces which do not come into contact with the liquid crystals 2.

Capacitors 12 and 13 as pixel capacitances are formed by the pixel electrode 6, and the opposite common electrode 7 and additional capacitance line 10, respectively. More specifically, as illustrated in Fig. 11, the capacitor 12 is formed by the pixel electrode 6 and the common electrode 7 to ensure a liquid crystal capacitance  $C_{LC}$ . In order to achieve

high image quality by improving the data retentivity of the liquid crystals 2, the capacitor 13 is formed by the pixel electrode 6 and the additional capacitance 10 to ensure an additional capacitance Cs.

In the liquid crystal display device of the above-mentioned structure, when scanning signals are successively input downward from the scanning drive circuit K to the scanning lines  $3_1, 3_2, \dots$ , the gates of a line of the TFTs 5 are simultaneously turned on, and display-use data signals are input to the signal lines  $4_1, 4_2, \dots$  for each pixel by the data drive circuit L. As a result, the data signals are input to the pixel electrodes 6, and the transmittance of the liquid crystals 2 is varied by the potential difference between the pixel electrodes 6 and the common electrodes 7.

In this case, when a direct current continues to be supplied over a long time, the data retentivity of the liquid crystals 2 deteriorates. Therefore, the liquid crystals 2 are driven by a so-called AC drive method in which a positive voltage and a negative voltage are alternately applied to the pixel electrode 6 by switching the polarity of the data signals to be input to the signal lines  $4_1, 4_2, \dots$ , for example, every horizontal scanning period.

In general, as an ideal capacitance (pixel capacitance) of a single pixel, only the liquid crystal capacitance  $C_{LC}$  and the additional capacitance  $C_s$  exist between the pixel electrode 6 and the common electrode 7 and between the pixel electrode 6 and the additional capacitance line 10, respectively, as shown in Fig. 11.

However, in actual fact, when conducting films are arranged parallel to each other, or the conducting films are placed one upon another with an insulating film therebetween, a parasitic capacitance is generated between the conducting films.

Therefore, for example, in a pixel located in the second row and the first column, i.e., a pixel in which the gate electrode 5g of the TFT 5 is connected to the second scanning line from the top,  $3_2$ , and the source electrode 5s is connected to the first signal line from the left,  $4_1$ , the periphery of the pixel electrode 6 is enclosed by the upper and lower scanning lines  $3_1$  and  $3_2$ , and the left and right signal lines  $4_1$  and  $4_2$  as shown in Fig. 9. Thus, in this pixel, as shown in Fig. 12, parasitic capacitances  $C_{gd_2}$ ,  $C_{gd_1}$ ,  $C_{sd_2}$ , and  $C_{sd_1}$  are generated between the pixel electrode 6 and the lines  $3_1$ ,  $3_2$ ,  $4_1$ , and  $4_2$ , respectively, as well as the liquid crystal

capacitance  $C_{LC}$  and the additional capacitance  $C_s$ .

The parasitic capacitance ratio in this pixel is given by

$$\alpha = \Delta C / (C_{LC} + C_s + \Delta C) \quad \dots \dots \quad (1)$$

where  $\Delta C = C_{gd_1} + C_{gd_2}$ .

When driving the liquid crystals 2 by the above-mentioned AC drive method, the parasitic capacitance ratio  $\alpha$  affects a fluctuation  $\Delta V$  of a voltage applied to the pixel electrode 6, and the voltage fluctuation  $\Delta V$  produces a DC component and deteriorates the data retentivity. Therefore, optimization is performed for each gray scale according to the parasitic capacitance ratio  $\alpha$  so as to prevent the generation of the DC component.

Next, with reference to a pixel in which the gate electrode 5g of the TFT 5 is connected to the topmost scanning line,  $3_1$ , shown in Fig. 1 from which the scanning of scanning signal starts and the source electrode 5s is connected to the first signal line,  $4_1$ , from the left, a parasitic capacitance ratio  $\alpha'$  in this pixel will be discussed.

Since the dummy scanning line  $3_0$  is arranged above the pixel electrode 6 constituting this pixel at the same pitch as the pitch of other adjacent scanning lines, for example,  $3_1$  and  $3_2$  so that the pixel

electrode 6 is located between the dummy scanning line 3<sub>0</sub> and the scanning line 3<sub>1</sub>, Ggd<sub>2</sub> is generated between the pixel electrode 6 and the dummy electrode 3<sub>0</sub> in the same manner as the above-mentioned parasitic capacitance generated between the pixel electrode 6 and the scanning line 3<sub>1</sub>.

Thus, the parasitic capacitance ratio in this pixel is given by

$$\alpha' = \Delta C' / (C_{Lc} + C_s + \Delta C') \dots \dots (2)$$

where  $\Delta C' = C_{gd_1} + C_{gd_2} = \Delta C$

Therefore,  $\alpha' = \Delta C / (C_{Lc} + C_s + \Delta C) = \alpha$

Namely, the pixel electrode 6 connected to the TFT 5 connected to the topmost scanning line 3<sub>1</sub> is sandwiched between the dummy scanning line 3<sub>0</sub> above and the scanning line 3<sub>1</sub> below. As a result, since all of the pixels are geometrically symmetrical about the additional capacitance line 10 as shown in Fig. 9, the parasitic capacitance ratio in all of the pixels becomes  $\alpha$  given by Equation (1) above, thereby preventing different parasitic capacitance ratios which are seen in a conventional structure.

Moreover, in this embodiment, a scanning signal G<sub>0</sub> having the same waveform and the same time difference  $\Delta T$  as normal scanning signals G<sub>1</sub>, G<sub>2</sub>, G<sub>3</sub>, ... to be input to the scanning lines 3<sub>1</sub>, 3<sub>2</sub>, ... by the scanning

drive circuit K is newly generated as shown in Fig. 2. The scanning signal  $G_0$  is applied to the dummy scanning line  $3_0$ , before an output of the scanning signal  $G_1$  to be applied to the topmost scanning line  $3_1$ . Hence, a part of the scanning drive circuit K forms signal input means for inputting a signal to the dummy scanning line  $3_0$ .

Thus, by performing optimization in advance according to the parasitic capacitance ratio  $\alpha$ , the pixel driven by the topmost scanning line  $3_1$  has completely the same conditions as the pixels driven by other scanning lines  $3_2, 3_3, \dots$ . Therefore, in the case of a normally white display, it is possible to completely eliminate such a conventional phenomenon that a line of pixels in the topmost row appears as a bright line.

It is arranged in this embodiment that the scanning of scanning signal starts from the topmost scanning line  $3_1$ . However, if the scanning of scanning signal is arranged to start from the lowest scanning line,  $3_i$ , the topmost scanning line  $3_1$  becomes the outermost scanning line on the scanning end side of scanning signal. Thus, the dummy scanning line  $3_0$  can be formed at the outermost position on either the scanning start side or the scanning end side of

scanning signal.

The following description will discuss the rate of occurrence of bright line in the liquid crystal display device of the above-mentioned structure.

With respect to the halftone display of a line of pixels corresponding to the topmost scanning line  $3_1$ , the rate of occurrence of bright line (relative value) was measured after continuously supplying a current under a temperature of  $60^{\circ}\text{C}$  for 6 hours and 240 hours. In Fig. 8, the block bar graph represents the rate of occurrence of bright line measured when 6 hours elapsed, while the white bar graph shows the value measured when 240 hours elapsed.

In this case, the rate of occurrence of bright line measured when six hours elapsed after successively inputting scanning signals  $G_1, G_2, \dots$  to the scanning lines  $3_1, 3_2, \dots$  without inputting any signal to the dummy scanning line  $3_0$ , was indicated as a reference value, 100.

In Fig. 8, (A) indicates the result obtained when the scanning signal  $G_0$  inherent in the dummy scanning line  $3_0$  was input. (D) shows the result obtained when any signal was not input to the dummy scanning line  $3_0$ .

It was found from these results that, when the scanning signal  $G_0$  shown in Fig. 2 was input to the

dummy scanning line  $3_0$ , such a phenomenon that only the topmost line appears as a bright line did not occur at all on the contrary to the case in which any signal was not input to the dummy scanning line  $3_0$ .

However, when the dummy scanning line  $3_0$  is not provided though this structure is not shown in Fig. 8, since the parasitic capacitance ratio certainly varies, the rate of occurrence of bright line becomes much higher than that in the above-mentioned case, (D), in which the dummy scanning line  $3_0$  is just provided. It was thus found that, even if a signal is not input to the dummy scanning line  $3_0$ , the rate of occurrence of bright line can be lowered to some degrees by just providing the dummy scanning line  $3_0$ .

[Embodiment 2]

The following description will discuss another embodiment of the present invention. The members having the same function as in Embodiment 1 above will be designated by the same code and their description will be omitted.

Like Embodiment 1, in a liquid crystal display device of this embodiment, as shown in Fig. 3, the dummy scanning line  $3_0$  for forming a capacitance is arranged outside of the topmost scanning line,  $3_1$ , on the scanning start side of scanning signal so that the

pixel electrode 6 connected to the TFT 5 connected to the scanning line  $3_1$  is located between the dummy scanning line  $3_0$  and the scanning line  $3_1$ .

However, in this embodiment, unlike Embodiment 1 above, the dummy scanning line  $3_0$  is connected to the lowest scanning line,  $3_i$ , through a coupling line 14. As a result, as shown in Fig. 4, a scanning signal  $G_i$  output to the lowest scanning line  $3_i$  from the scanning drive circuit K is directly input to the dummy scanning line  $3_0$  through the coupling line 14.

In this case, since the scanning signal  $G_0$  input to the dummy scanning line  $3_0$  is the scanning signal  $G_i$  output to the scanning line  $3_i$ , the scanning signal  $G_0$  certainly has the same waveform and the same time difference  $\Delta T$  as the normal scanning signals  $G_1$ ,  $G_2$ ,  $G_3$ , ... input to the scanning lines  $3_1$ ,  $3_2$ , ... by the scanning drive circuit K. Consequently, there is no need to newly generate the scanning signal  $G_0$  to be input to the dummy scanning line  $3_0$ . Namely, the scanning drive circuit K functions as the signal input means for inputting a signal to the dummy scanning line  $3_0$ .

Therefore, in this structure, unlike Embodiment 1, the existent scanning signal  $G_i$  can be used without newly generating the scanning signal  $G_0$  inherent in the

dummy scanning line  $3_0$  by changing a part of the scanning drive circuit K. Moreover, since the time difference between the output of the scanning signal  $G_i$  and the output of the scanning signal  $G_1$  to be applied to the topmost scanning line  $3_1$  is the smallest, the pixels driven by the topmost scanning line  $3_1$  have substantially the same conditions as the pixels driven by other scanning lines  $3_2, 3_3, \dots$ , thereby reducing defects, such as the phenomenon in which a line of pixels appear as a bright line, to a sufficient level.

Thus, when the scanning signal  $G_i$  to be applied to the lowest scanning line  $3_i$  is input to the dummy scanning line  $3_0$ , as shown in (A) of Fig. 8, the rate of occurrence of bright line becomes zero. This means that the phenomenon in which only the topmost line appears as a bright line is completely eliminated.

However, in this embodiment, since the display mode of the liquid crystal display device is the SVGA mode, the vertical blanking period is about 10 % of one field. Therefore, the output of a scanning signal to each scanning line is shifted from each other by about one tenth of a field as shown in Fig. 4.

[Embodiment 3]

The following description will discuss still

another embodiment of the present invention. The members having the same function as in Embodiment 1 will be designated by the same code and their description will be omitted.

Like Embodiment 1 above, in a liquid crystal display device of this embodiment, as shown in Fig. 5, the dummy scanning line  $3_0$  for forming a capacitance is arranged outside of the topmost scanning line,  $3_1$ , on the scanning start side of scanning signal so that the pixel electrode 6 connected to the TFT 5 connected to the scanning line  $3_1$  is placed between the dummy scanning line  $3_0$  and the scanning line  $3_1$ .

However, in this embodiment, unlike Embodiment 1, the dummy scanning line  $3_0$  is connected to the common line 9 through a coupling line 15. As a result, as shown in Fig. 6, a common signal  $V_{com}$  to be applied to the common line 9 is directly input to the dummy scanning line  $3_0$  through the coupling line 15. Namely, means for generating the common signal  $V_{com}$  functions as the signal input means for inputting a signal to the dummy scanning line  $3_0$ .

More specifically, since the common signal  $V_{com}$  which switches its level every horizontal scanning period (1H) is input through the common line 9 to the common electrode 7 and the additional capacitance line

10 in order to drive the liquid crystals 2 by the AC drive method, the common signal  $V_{com}$  is simultaneously input to the scanning lines and the dummy scanning line  $3_0$ .

Therefore, in this structure, the existent common signal  $V_{com}$  can be used without newly generating the scanning signal  $G_0$  inherent in the dummy scanning line  $3_0$  by changing a part of the scanning drive circuit K like Embodiment 1.

Moreover, the rate of occurrence of bright line when the common signal  $V_{com}$  (see Fig. 6) was input to the dummy scanning line  $3_0$  is the one shown in (C) of Fig. 8. It was found from this result that, when the common signal  $V_{com}$  is input to the dummy scanning line  $3_0$ , the rate of occurrence of bright line can be reduced to about a half of the rate (shown in (D) of Fig. 8) measured when any signal was not input to the dummy scanning line  $3_0$ .

[Embodiment 4]

The following description will discuss yet another embodiment of the present invention. In this embodiment, a liquid crystal display device having the same circuit structure as in Embodiment 1 is used.

In this embodiment, as shown in Fig. 7, the scanning signal  $G_0$  of a low level that cannot turn on

the TFT 5, for example, in a range of -7.5 V to -2.5 V, is input to the dummy scanning line  $3_0$ . This low level scanning signal  $G_0$  is generated in the scanning drive circuit K. Namely, means for inputting a signal to the TFT 5 functions as the signal input means for inputting a signal to the dummy scanning line  $3_0$ .

Therefore, the rate of occurrence of bright line when the scanning signal  $G_0$  shown in Fig. 7 was input to the dummy scanning line  $3_0$  is the one shown in (B) of Fig. 8. It was found from this result that, when the scanning signal  $G_0$  is input to the dummy scanning line  $3_0$ , the rate of occurrence of bright line can be reduced to about a half of the rate (shown in (D) of Fig. 8) measured when any signal was not input to the dummy scanning line  $3_0$ .

[Embodiment 5]

The following description will discuss another embodiment of the present invention. In this embodiment, a liquid crystal display device having the same circuit structure as in Embodiment 1 is used.

In this embodiment, in the above-mentioned liquid crystal display device, any one of the scanning signals to be input to the scanning lines  $3_1$ ,  $3_2$ , ... is input as the scanning signal  $G_0$  to the dummy scanning line  $3_0$ . In this case, like Embodiment 2, the

scanning drive circuit K functions as the signal input means for inputting a signal to the dummy scanning lines  $3_0$ .

For example, the rate of occurrence of bright line was measured when the scanning signal  $G_2$  to be input to the scanning line  $3_2$  in the second row was input as the scanning signal  $G_0$  to the dummy scanning line  $3_0$ . It was found from this result that the rate of occurrence of bright line becomes zero as shown in (A) of Fig. 8. Namely, a phenomenon in which only the topmost line appears as a bright line is completely eliminated.

[Embodiment 6]

The following description will discuss another embodiment of the present invention. The members having the same function as in Embodiment 1 above will be designated by the same code and their description will be omitted.

Unlike the liquid crystal display device of Embodiment 1, in a liquid crystal display device of this embodiment, as shown in Fig. 13, the pixel electrode 6 is formed so that the pixel electrode 6 partly overlaps the dummy scanning line  $3_0$ , the scanning line  $3_1$ , the signal lines  $4_1$  and  $4_2$ .

For example, as illustrated in Fig. 14, an inter-

layer insulating film 21 is formed by an insulating resin or the like to cover the TFT 5 on the lower glass substrate 1a, the scanning line connected to the gate electrode 5g of the TFT 5, and the signal line connected to the source electrode 5s of the TFT 5. A contact hole 21a is formed in the inter-layer insulating film 21 at a position corresponding to the drain electrode 5d of the TFT 5.

The pixel electrode 6 is formed on the inter-layer insulating film 21 so that the pixel electrode 6 is electrically connected to the drain electrode 5d of the TFT 5 through the contact hole 21a, and partly overlaps the dummy scanning line 3<sub>0</sub>, the scanning line 3<sub>1</sub>, the signal lines 4<sub>1</sub> and 4<sub>2</sub>. Similarly, the pixel electrodes 6 connected in the vicinity of the intersections of other scanning lines and signal lines partly overlap the dummy scanning lines, the scanning lines and the signal lines.

By forming the inter-layer insulating film 21 on the dummy scanning line 3<sub>0</sub>, the scanning lines 3<sub>1</sub>, ... and the signal lines 4<sub>1</sub>, 4<sub>2</sub>, ... and successively forming the pixel electrodes 6 on the inter-layer insulating film 21 so that the pixel electrodes 6 overlap the respective lines, it is possible to increase the aperture ratio and reduce alignment

defects of liquid crystals, resulting in improved quality.

Moreover, in the structure in which the pixel electrodes 6 overlap the respective lines, the parasitic capacitance between a pixel and adjacent scanning line is increased to a value which is about twice that of a structure having no inter-layer insulating film 21, i.e., a structure in which the pixel electrodes 6 do not overlap the respective lines (for example, the structure shown in Fig. 9), and defects, such as the phenomenon in which the topmost scanning line 3<sub>1</sub> appears as a bright line, tend to increase.

However, in this embodiment, the dummy scanning line 3<sub>0</sub> is arranged outside of the topmost scanning line, 3<sub>1</sub>, parallel to the scanning line 3<sub>1</sub>, and the pixel electrode 6 overlaps the dummy scanning line 3<sub>0</sub> with the inter-layer insulating film 21 therebetween. Therefore, even if the parasitic capacitance is increased to a value which is about twice that of the structure shown in Fig. 9, all of the pixels are geometrically symmetrical about the additional capacitance line 10. As a result, the parasitic capacitance ratio is equalized in all of the pixels, thereby certainly preventing defects, such as the

occurrence of bright line due to different parasitic capacitance ratios.

Thus, in the liquid crystal display device of this embodiment, it is possible to increase the aperture ratio, restrain the alignment defects of liquid crystals, reduce the occurrence of defects such as the appearance of bright line, and achieve improved quality.

In addition, the rate of occurrence of bright line can further be reduced by inputting some signal to the dummy scanning line  $3_0$  of the liquid crystal display device of the above-mentioned structure. For instance, by inputting the scanning signal  $G_0$  shown in Fig. 2 of Embodiment 1, it is possible to completely prevent the occurrence of bright line. Even when the scanning signal  $G_0$  described in other embodiment is input, it is possible to completely prevent or reduce the occurrence of bright line.

In the above-mentioned embodiments, 1 to 6, a line of pixels corresponding to the topmost scanning line  $3_1$  may be hidden with a light blocking pattern, instead of providing the dummy scanning line  $3_0$ , so as to prevent this line of pixels from affecting the display. However, in this state, if a current continues to be supplied over a long time, the

appearance of bright line in the first row may gradually spread to the second row. Thus, this structure is not an appropriate measure to prevent the defects.

Therefore, in the structure where the first line of pixels is shaded from light, if the dummy scanning line  $3_0$  is provided like the present invention, it is possible to prevent the second line of pixels from appearing as a bright line.

Furthermore, in Embodiments 1 to 6, the dummy scanning line  $3_0$  is arranged outside of the topmost scanning line  $3_1$ . However, the present invention is not limited to this structure. For instance, when the scanning of scanning signal starts from the lowest scanning line  $3_i$ , a dummy scanning line  $3_{i+1}$  is arranged outside of the lowest scanning line  $3_i$ .

In the liquid crystal display device of the present invention, an inter-layer insulating film covering the top of switching elements, scanning lines and signal lines is formed, and pixel electrodes are formed so that the pixel electrodes overlap the dummy scanning line and the adjacent scanning line corresponding to the pixel electrodes with the inter-layer insulating film therebetween.

Consequently, since the aperture ratio is

improved and the alignment defect of liquid crystals is reduced as described above, it is possible to achieve a highly reliable liquid crystal display device.

Moreover, a drive method of the liquid crystal display device of the present invention includes the step of inputting a signal to the dummy scanning line formed outside of the outermost scanning line on either the scanning start side or the scanning end side of scanning signal.

Thus, by providing a dummy scanning line and inputting a signal to the dummy scanning line, the symmetry of the scanning line located on the outermost position on the scanning start side of scanning signal and the dummy scanning line about the additional capacitance line and the symmetry of other adjacent scanning lines about the additional capacitance line are substantially equalized, thereby ensuring higher display quality.

Additionally, the liquid crystal display devices of Embodiments 1 to 6 have a so-called Cs on Com structure in which the additional capacitance Cs between the pixel electrode 6 and the additional capacitance line 10 is formed on the common line 9. Hence, such a liquid crystal display device can be

easily driven. Furthermore, in the Cs on Com structure, since the parasitic capacitance between the gate and source lines is reduced, it is possible to decrease shadowing (particularly in a lateral direction (scanning direction)). Consequently, the present invention can achieve a liquid crystal display device which is easily driven and has high display quality as well as the effect (an improvement of reliability) produced by the above-mentioned dummy scanning line.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A liquid crystal display device comprising:
  - a pair of substrates sandwiching liquid crystals therebetween;
  - a plurality of scanning lines to which scanning signals are successively applied;
  - a plurality of signal lines to which data signals are successively applied, said signal lines intersecting said scanning lines at right angles;
  - a switching element which is arranged in a vicinity of each of intersections of said scanning lines and said signal lines, and electrically connected to both of said scanning and signal lines;
  - a pixel electrode connected to each of said switching elements;
  - said scanning lines, signal lines, switching elements and pixel electrodes being formed on one of said substrates,
  - a common electrode formed on the other of said substrates so that said common electrode faces said pixel electrode with said liquid crystals therebetween;
  - a common line for supplying a common signal to said common electrode;
  - a pixel capacitance, one of electrodes of said

pixel capacitance formed by said pixel electrode being connected to said common line; and

a dummy scanning line formed outside of one of said scanning lines located at an outermost position on either a scanning start side or a scanning end side of scanning signal.

2. The liquid crystal display device according to claim 1,

wherein said dummy scanning line is arranged at a pitch equal to a pitch of other adjacent scanning lines so that said pixel electrode is located between said dummy scanning line and the scanning line located at the outermost position.

3. The liquid crystal display device according to claim 1,

wherein an inter-layer insulating film is formed over said switching elements, scanning lines and signal lines, and

each of said pixel electrodes overlaps said dummy scanning line and adjacent scanning line corresponding to said pixel electrode with said inter-layer insulating film therebetween.

4. The liquid crystal display device according to claim 1, further comprising signal input means for inputting a signal to said dummy scanning line.

5. The liquid crystal display device according to claim 4,

wherein said signal input means inputs a signal to said dummy scanning line before an output of a scanning signal to be input to the scanning line located at the outermost position on the scanning start side of scanning signal.

6. The liquid crystal display device according to claim 4,

wherein said signal input means inputs a signal to said dummy scanning line after an output of a scanning signal to be input to the scanning line located at the outermost position on the scanning end side of scanning signal.

7. The liquid crystal display device according to claim 4,

wherein said signal input means inputs a scanning signal generated exclusively for said dummy scanning line to said dummy scanning line.

8. The liquid crystal display device according to claim 4,

wherein said signal input means inputs to said dummy scanning line a scanning signal to be input to the scanning line located at the outermost position on either the scanning start side or the scanning end side of scanning signal.

9. The liquid crystal display device according to claim 4,

wherein said signal input means inputs to said dummy scanning line the common signal to be input to said common electrode.

10. The liquid crystal display device according to claim 4,

wherein said signal input means inputs to said dummy scanning line a scanning signal of a level which does not turn on said switching elements formed on said substrate.

11. A method of driving a liquid crystal display device including a plurality of scanning line to which scanning signals are successively applied, a plurality of signal lines to which data signals are successively

applied, a switching element which is arranged in a vicinity of each of intersections of the scanning lines and the signal lines and connected to both of the scanning and signal lines, a pixel electrode connected to each of the switching element, a pixel capacitance formed by the pixel electrode, a common electrode which is arranged to face the pixel electrode, liquid crystals placed between the pixel electrode and the common electrode, and a dummy scanning line formed outside of one of the scanning lines located at an outermost position on either a scanning start side or a scanning end side of scanning signal, said method comprising the steps of:

supplying the scanning signal and the data signal to the switching element and supplying a common signal to one of electrodes of the pixel capacitance so as to change an electric potential between the pixel electrode and the common electrode and vary a transmittance of the liquid crystals; and  
inputting a signal to the dummy scanning line.

12. The method of driving the liquid crystal display device according to claim 11,

wherein the signal to be input to the dummy scanning line is output before an output of a scanning

signal to be input to the scanning line located at the outermost position on the scanning start side of scanning signal.

13. The method of driving the liquid crystal display device according to claim 11,

wherein the signal to be input to the dummy scanning line is output after an output of a scanning signal to be input to the scanning line located at the outermost position on the scanning end side of scanning signal.

14. The method of driving the liquid crystal display device according to claim 11,

wherein the signal to be input to the dummy scanning line is a scanning signal generated exclusively for the dummy scanning line.

15. The method of driving the liquid crystal display device according to claim 11,

wherein the signal to be input to the dummy scanning line is a scanning signal to be input to the scanning line located at the outermost position on either the scanning start side or the scanning end side of scanning signal.

16. The method of driving the liquid crystal display device according to claim 11,

wherein the signal to be input to the dummy scanning line is the common signal to be applied to the common electrode.

17. The method of driving the liquid crystal display device according to claim 11,

wherein the signal to be input to the dummy scanning line is a scanning signal of a level which does not turn on the switching elements.

## ABSTRACT OF THE DISCLOSURE

A liquid crystal display device is formed by arranging a plurality of scanning lines  $3_1, 3_2, \dots$  to which scanning signals are successively applied and a plurality of signal lines  $4_1, 4_2, \dots$  to which data signals are successively applied to intersect at right angles. Mounted in the vicinity of each of the intersections of the scanning lines  $3_1, 3_2, \dots$  and signal lines  $4_1, 4_2, \dots$  are a TFT 5 electrically connected to both of the lines, and a pixel electrode 6 connected to the TFT 5. A common electrode is placed to face the pixel electrode 6 with liquid crystals 2 therebetween. One of electrodes of a pixel capacitance formed by the pixel electrode 6 is connected to a common line 9 for supplying a common signal to the common electrode 7. A dummy scanning line  $3_0$  for forming a capacitance is arranged outside of the scanning line  $3_1$  located at the outermost position on a scanning start side of scanning signal. In this structure, since an equal parasitic capacitance is generated in the pixels irrespectively of their positions, it is possible to eliminate defects, such as deterioration of display quality due to an appearance of a bright line in particular pixels.

FIG.1

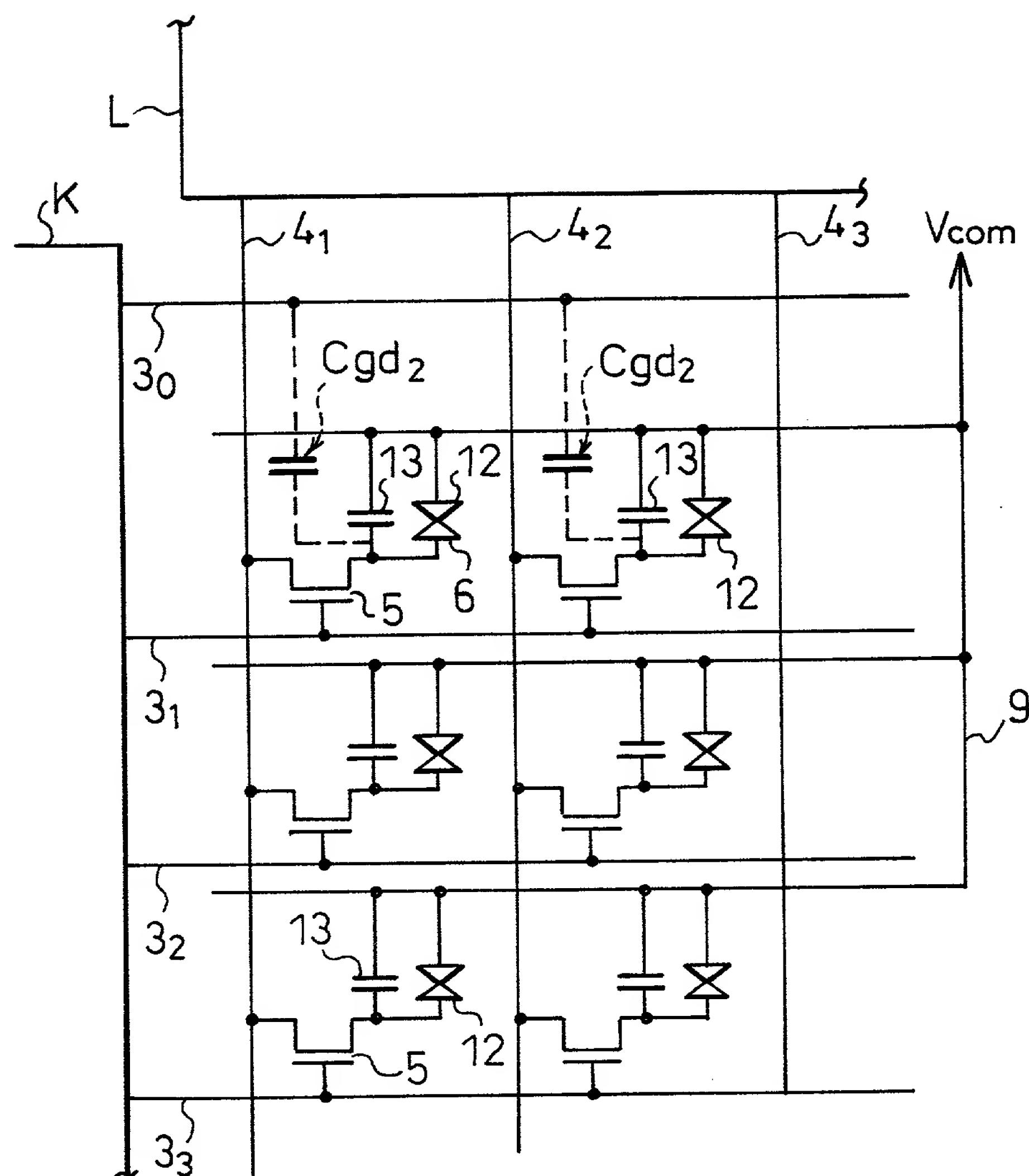


FIG.2

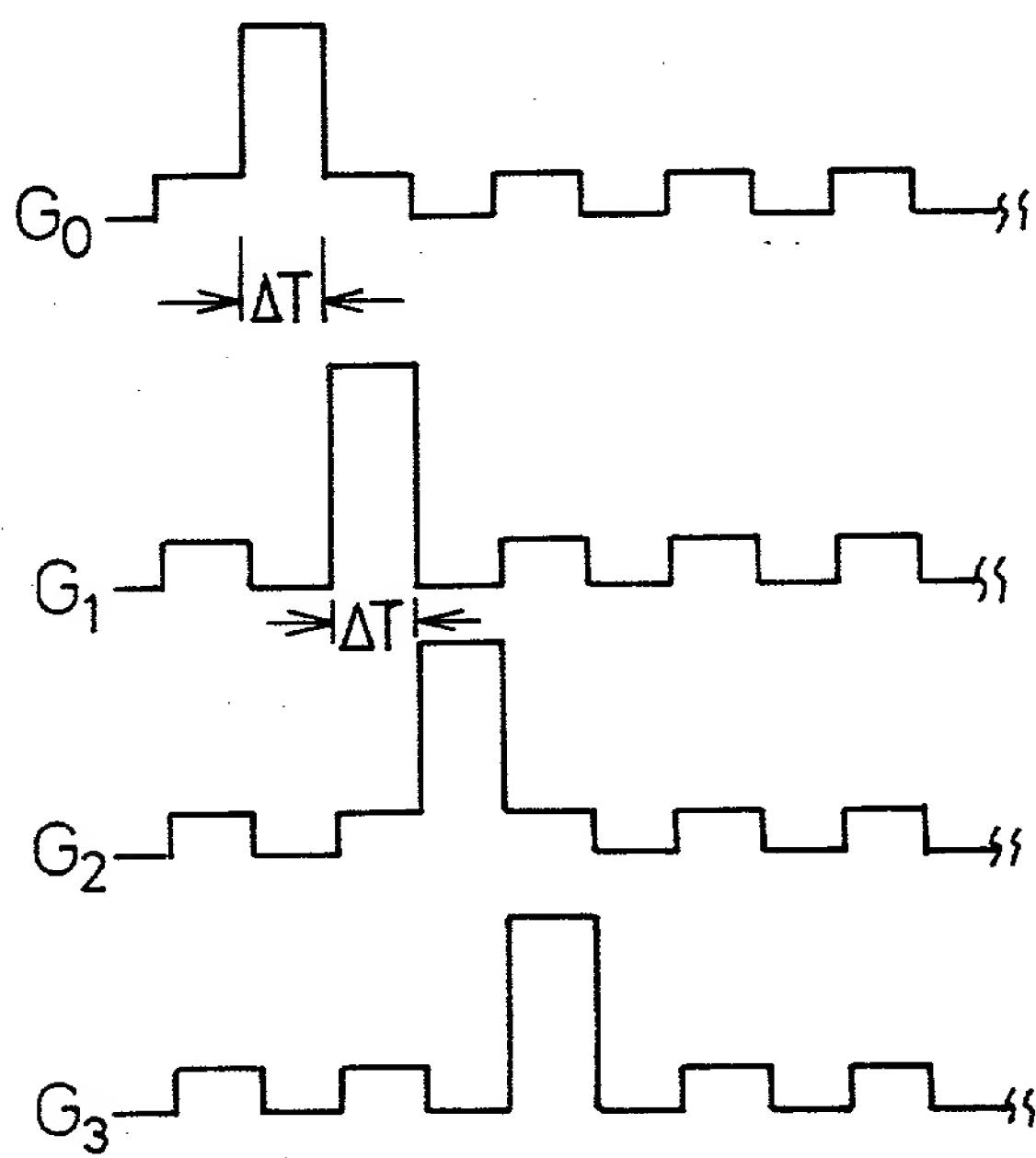


FIG. 3

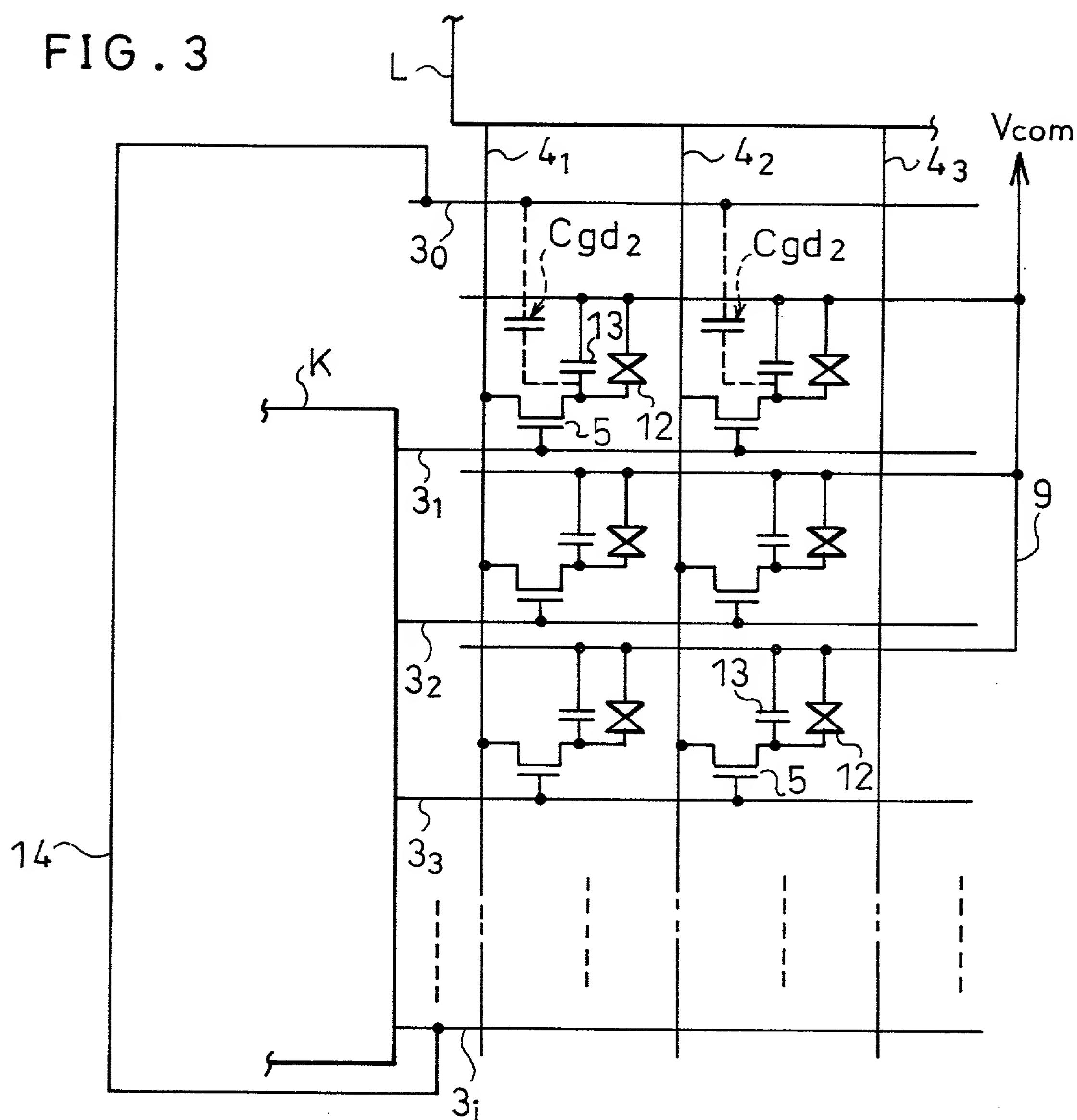
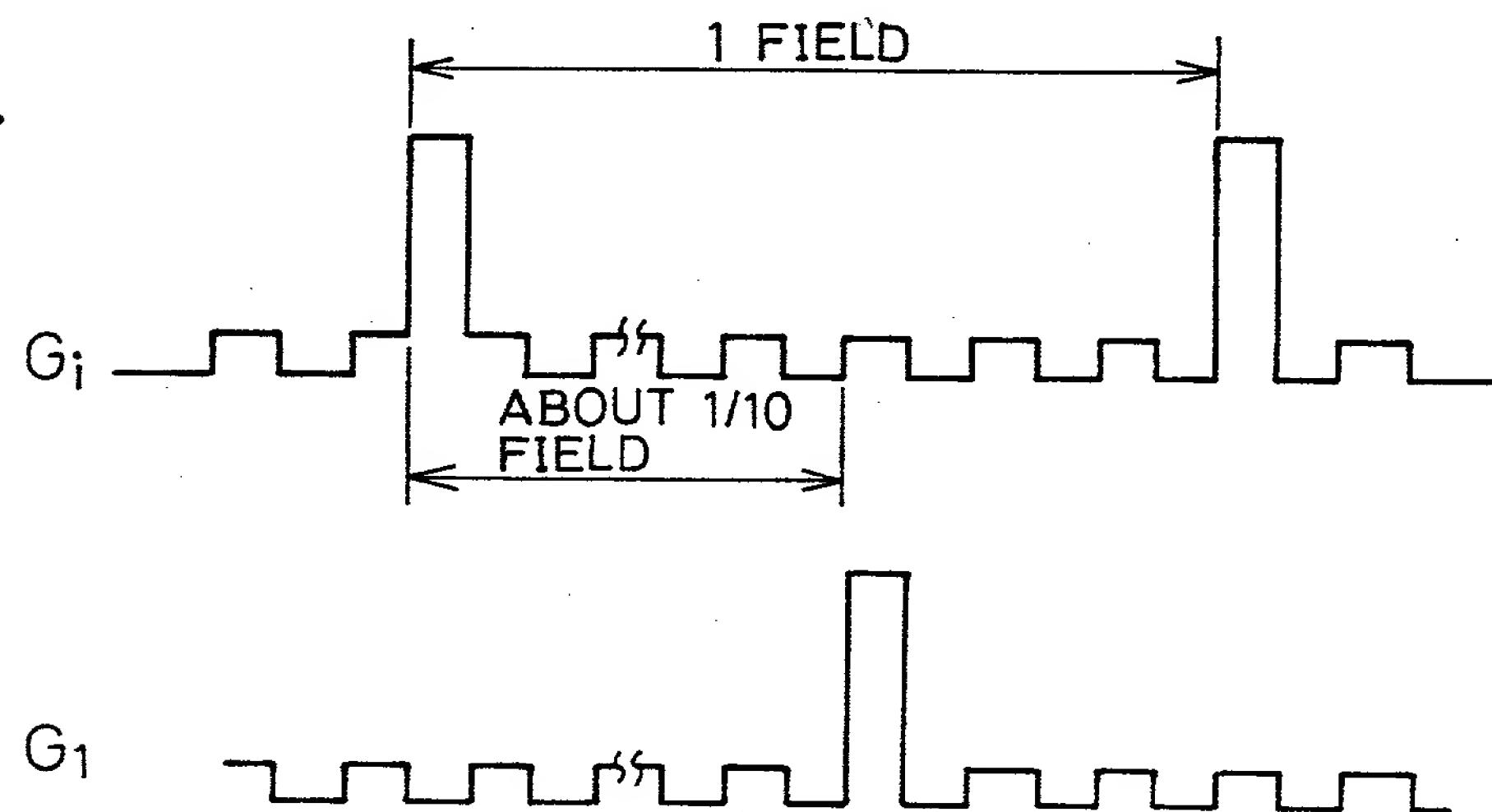
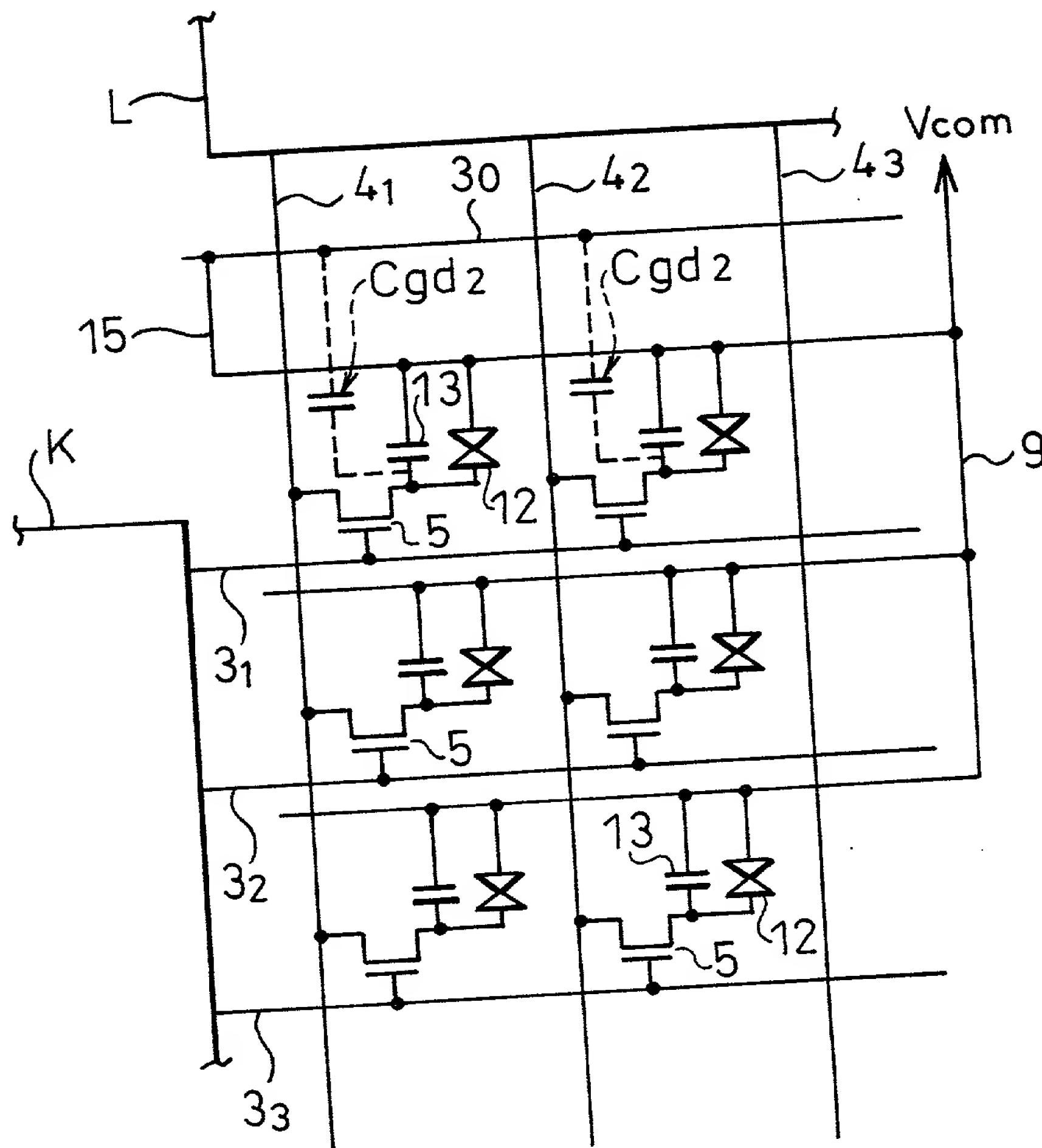


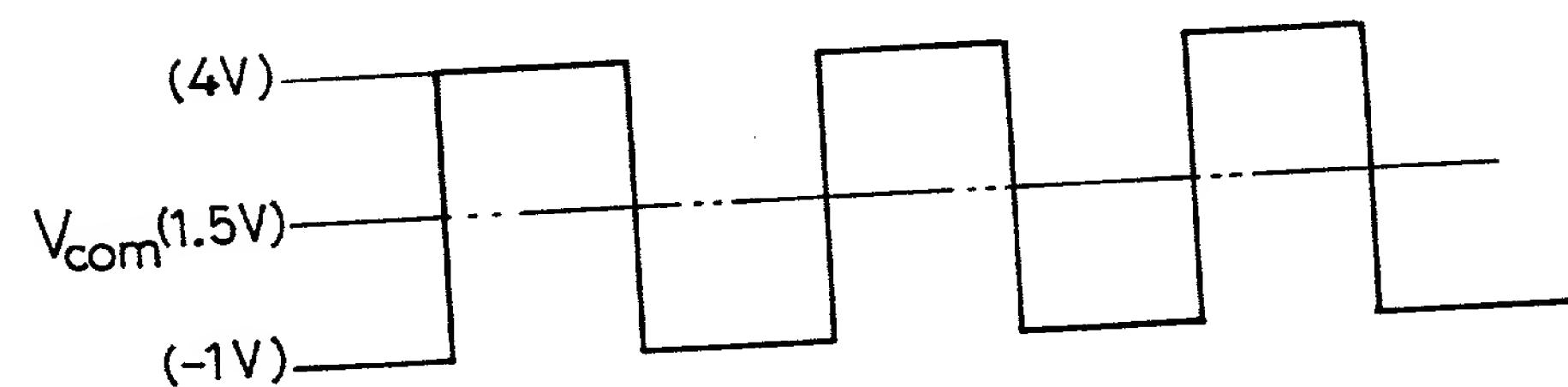
FIG. 4



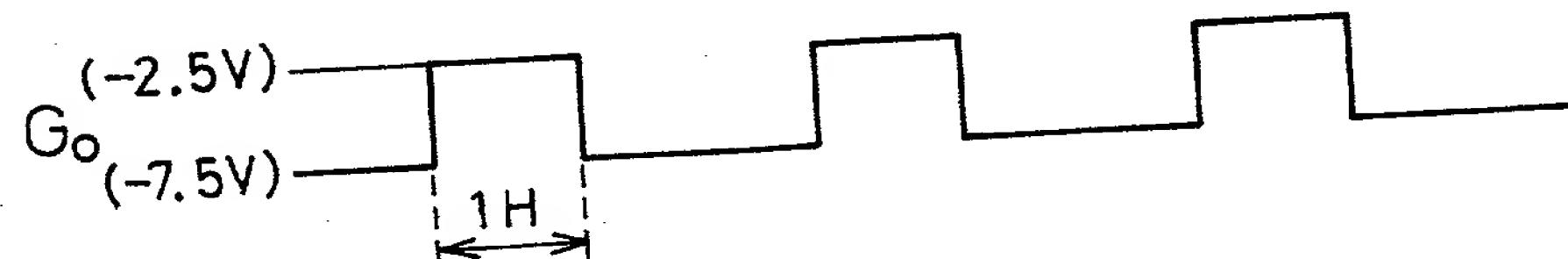
**FIG.5**



**FIG.6**



**FIG.7**



**FIG. 8**



FIG. 9

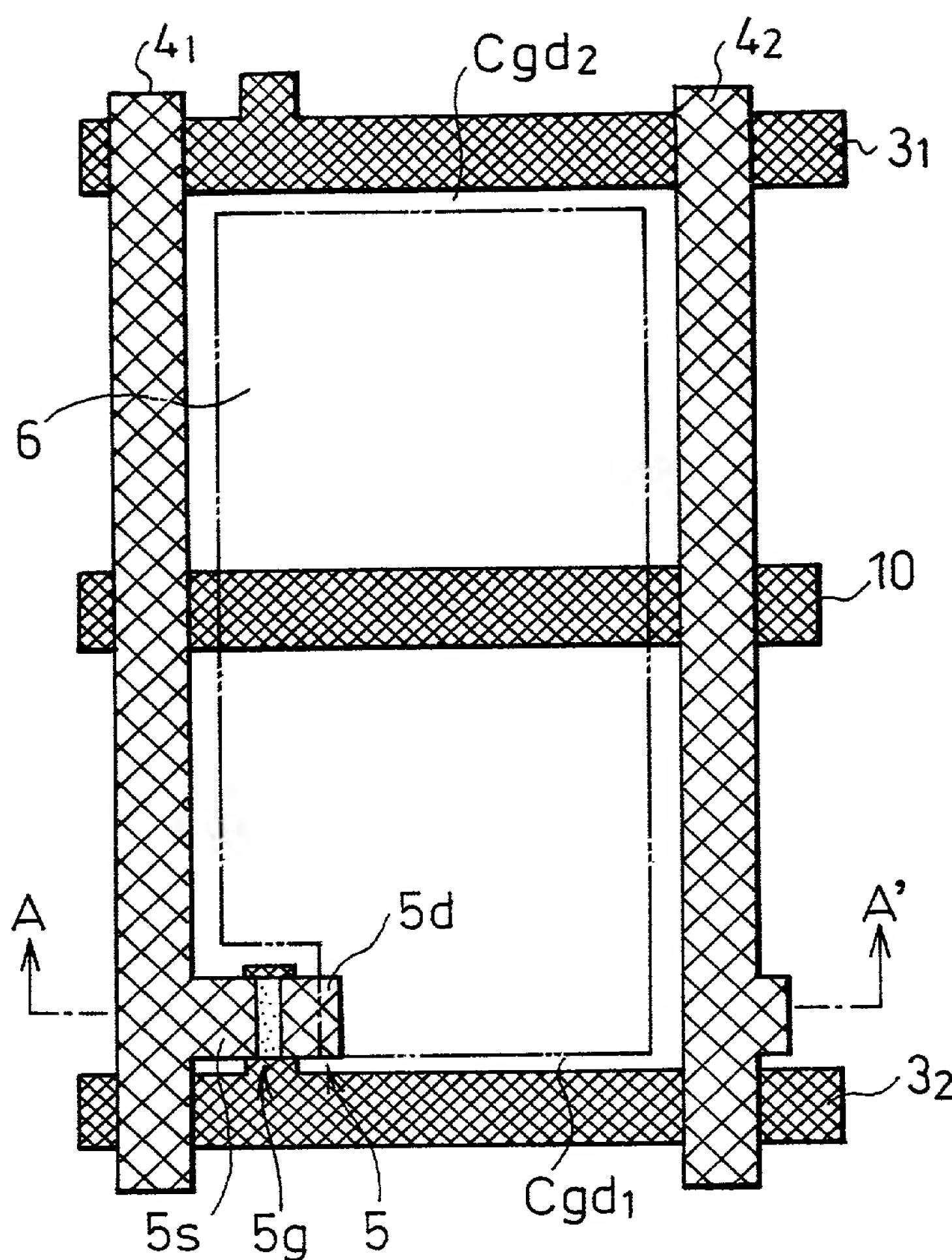


FIG. 10

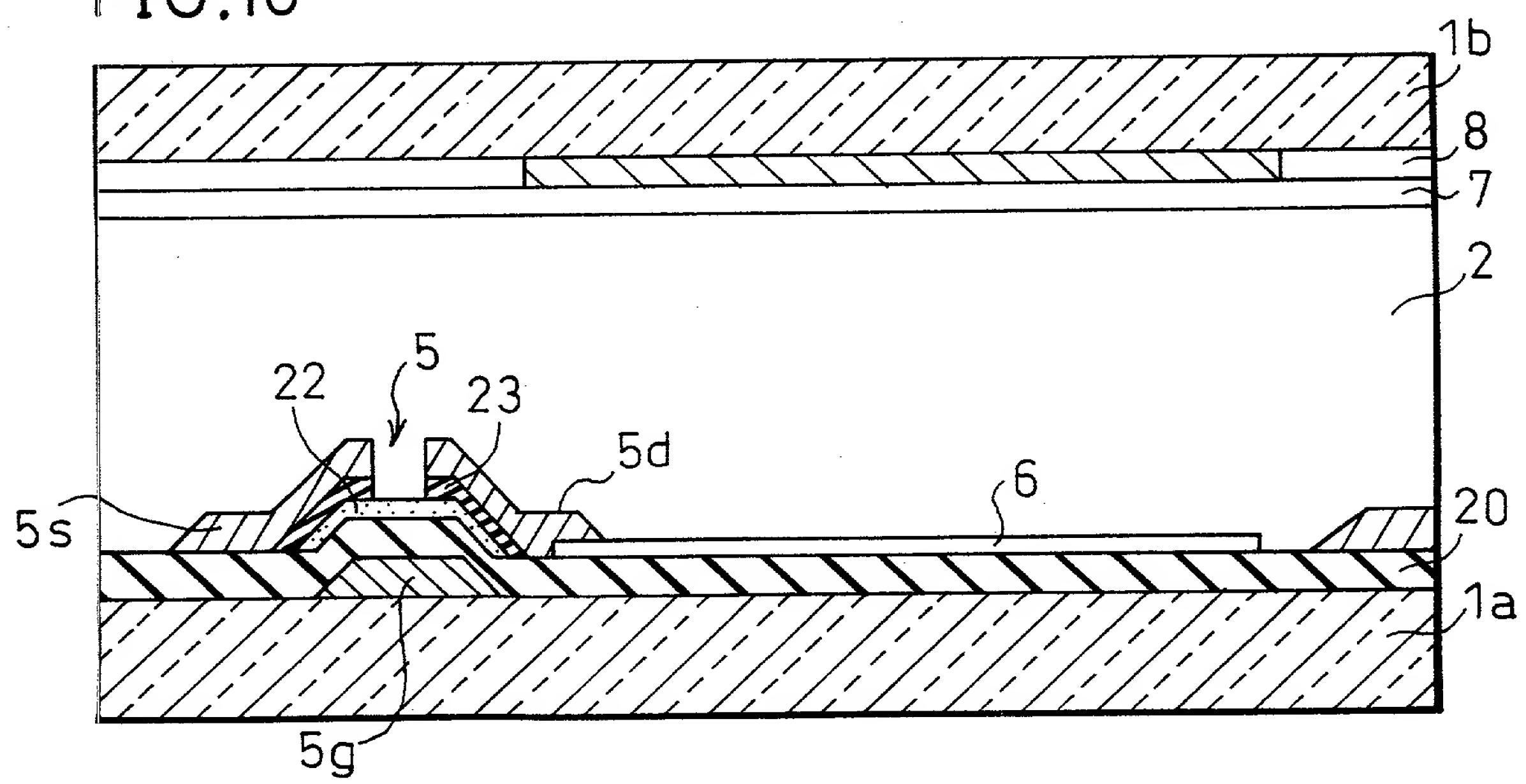


FIG.11

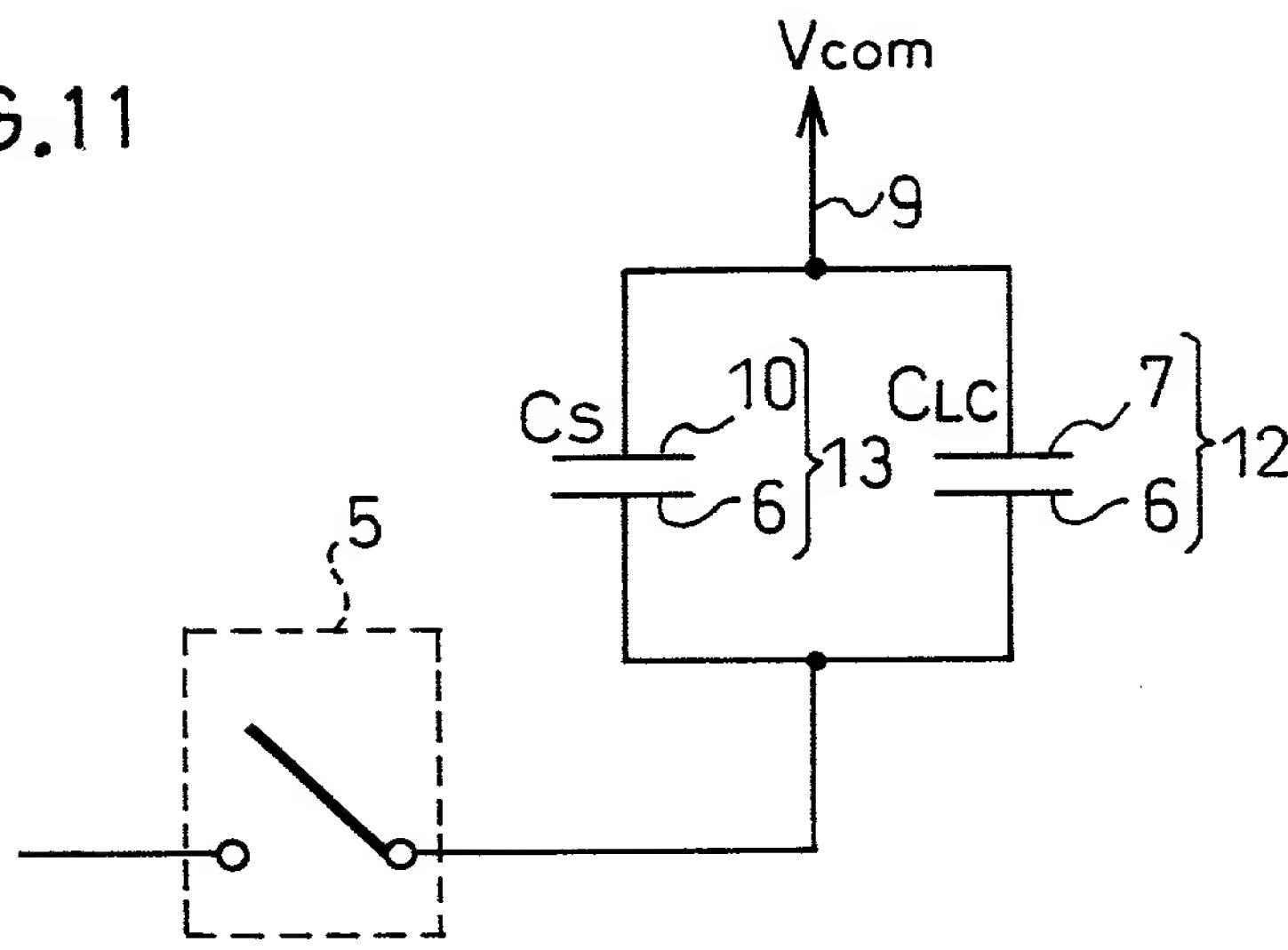


FIG.12

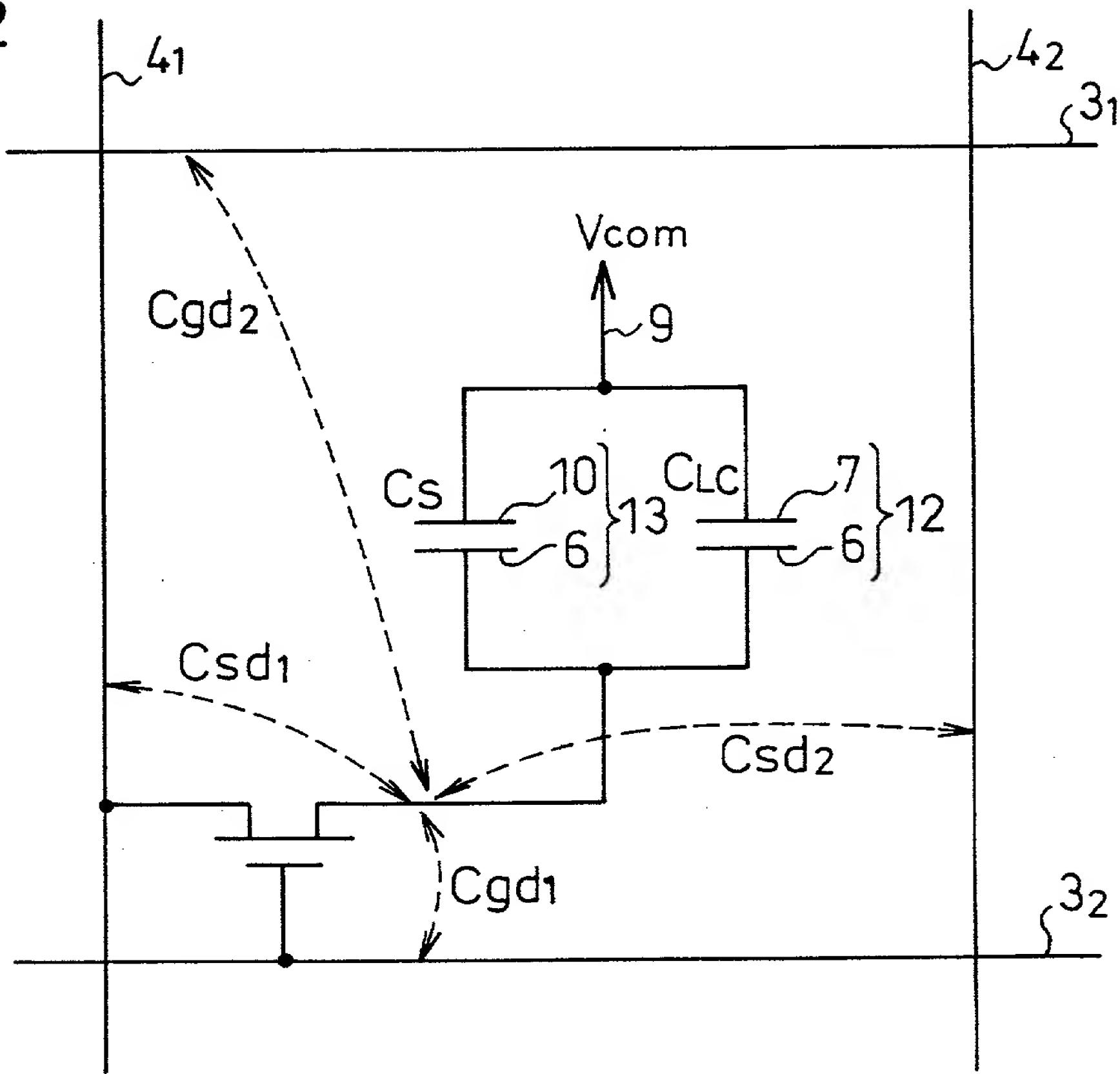


FIG.13

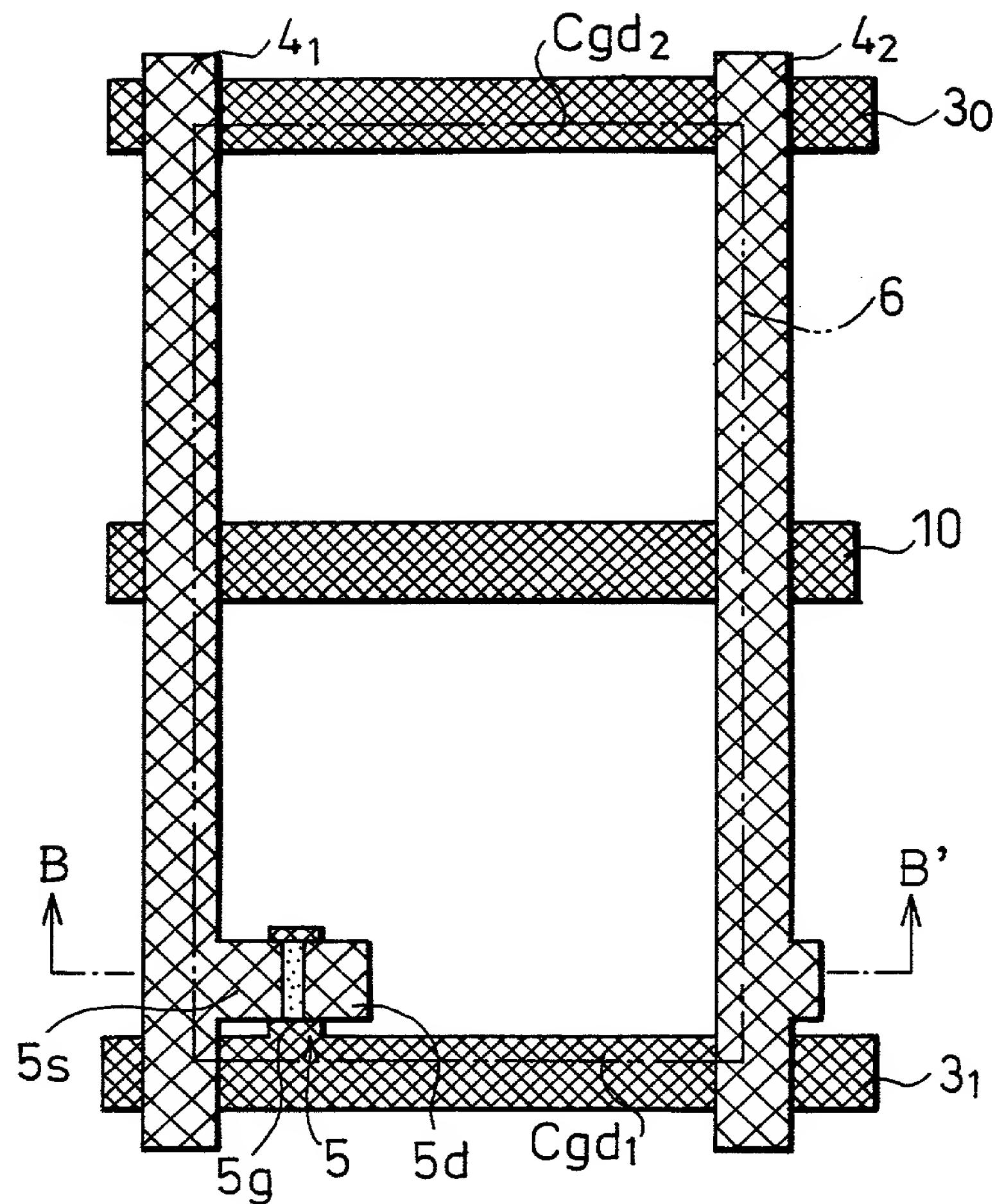


FIG.14

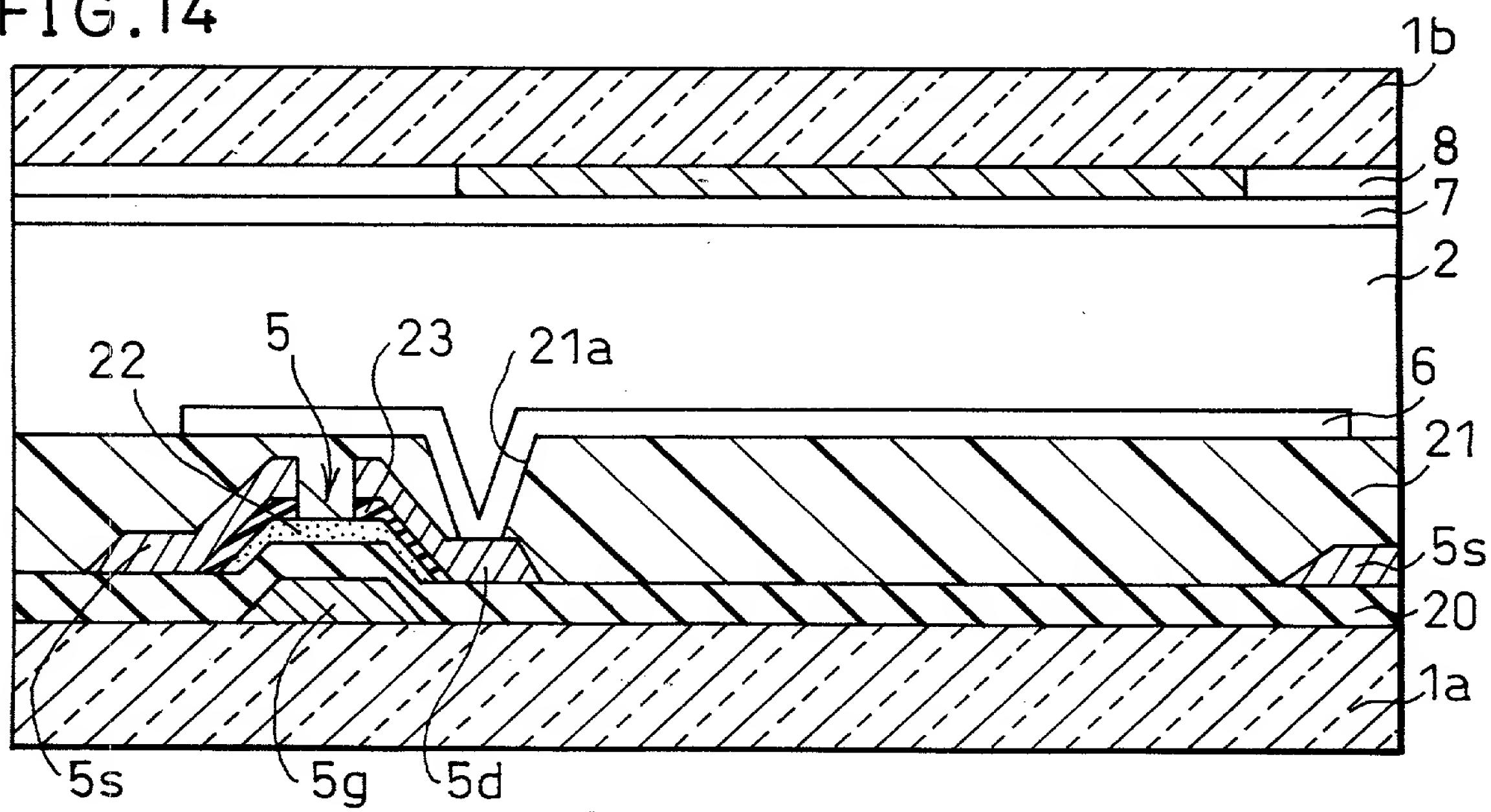
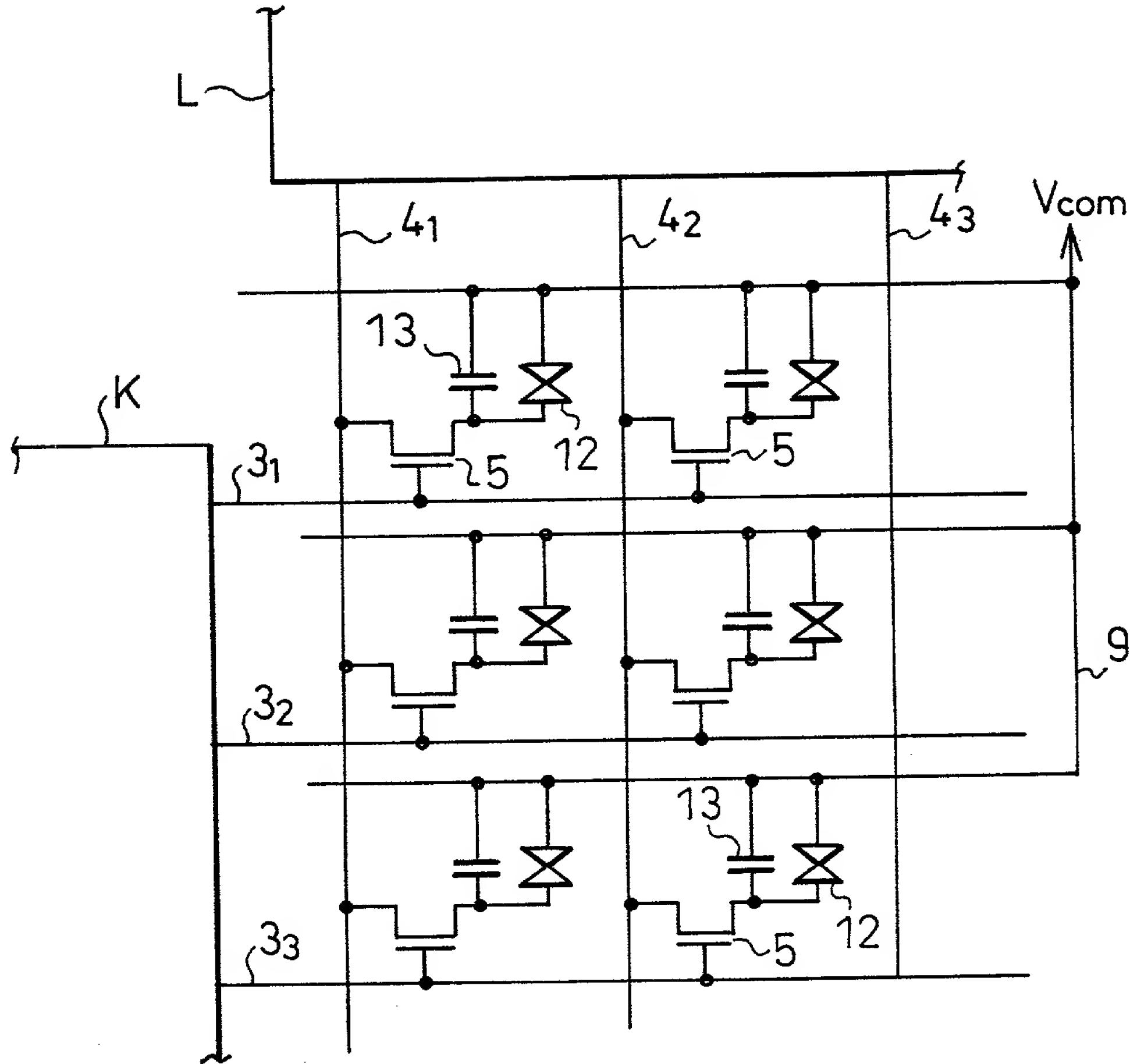


FIG.15



RULE 63 (37 C.F.R. 1.63)  
 DECLARATION AND POWER OF ATTORNEY  
 FOR PATENT APPLICATION  
 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Nixon & Vanderhye P.C. (6/92)

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled Liquid Crystal Display Device and Method of Driving the Same

the specification of which (check applicable box(es)):

is attached hereto.

was filed on \_\_\_\_\_ as U.S. Application Serial No. \_\_\_\_\_

was filed as PCT international application No. PCT/\_\_\_\_\_ on \_\_\_\_\_ and (if applicable to U.S. or PCT application) was amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. 1.56(a). I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Prior Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
8-100073	Japan	22/Apr./1996

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56(a) which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s):

Application Serial No.	Day/Month/Year Filed	Status: patented, pending, abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint NIXON & VANDERHYE P.C., 1100 North Glebe Road, 8th Floor, Arlington, Virginia 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed), and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Fatis, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Paul J. Henon, 33626; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr., 29366; Thomas E. Byrne, 32205.

1) Inventor's Signature Shinya Tanaka Date March 28, 1997

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3) Inventor's Signature Takashi Ochi Date March 28, 1997

Inventor's Name (typed)	<u>Takashi</u>	OCHI	Japanese
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First	Middle Initial	Family Name	Citizenship

Residence (City)	(State/Foreign Country)	<u>Nara Japan</u>
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Post Office Address	<u>2613-1, Ichinomoto-cho Tenri-shi Nara Japan</u>	Zip Code	<u>632</u>
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FOR ADDITIONAL INVENTORS, check box [X] and attach sheet with same information and signature and date for each.

RULE 63 (37 C.F.R. 1.63)  
**DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION  
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Nixon & Vanderhye P.C. (6/92)

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled \_\_\_\_\_

**LIOUID CRYSTAL DISPLAY DEVICE AND METHOD OF DRIVING THE SAME**

the specification of which (check applicable box(es)): \_\_\_\_\_

[ X ] is attached hereto.

[ ] was filed on \_\_\_\_\_ as U.S. Application Serial No. \_\_\_\_\_

[ ] was filed as PCT international application No. PCT/\_\_\_\_\_ on \_\_\_\_\_

and (if applicable to U.S. or PCT application) was amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. 1.56(a). I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

**Prior Foreign Application(s):**

Application Number	Country	Day/Month/Year Filed
8-100073	Japan	22/Apr./1996

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56(a) which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

**Prior U.S./PCT Application(s):**

Application Serial No.	Day/Month/Year Filed	Status: patented, pending, abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint NIXON & VANDERHYE P.C., 1100 North Glebe Road, 8th Floor, Arlington, Virginia 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed), and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Paul J. Henon, 33626; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr., 29366; Thomas E. Byrne, 32205.

1) Inventor's Signature Yuzuru Kanemori Date March 28, 1997

Inventor's Name (typed)	Yuzuru	KANEMORI	Japanese
First	Middle Initial	Family Name	Citizenship

Residence (City)	Nara-shi	(State/Foreign Country)	Nara Japan
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Post Office Address	3-2-201, 3-chome Daianji Nara-shi Nara Japan	Zip Code	630
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2) Inventor's Signature Mikio Katayama Date March 28, 1997

Inventor's Name (typed)	Mikio	KATAYAMA	Japanese
First	Middle Initial	Family Name	Citizenship

Residence (City)	Ikoma-shi	(State/Foreign Country)	Nara Japan
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Post Office Address	19-15, 4-chome Kitayamato Ikoma-shi Nara Japan	Zip Code	630-01
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3) Inventor's Signature \_\_\_\_\_ Date \_\_\_\_\_

Inventor's Name (typed)		First	Middle Initial	Family Name	Citizenship
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Residence (City)		(State/Foreign Country)	
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Post Office Address		Zip Code	
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FOR ADDITIONAL INVENTORS, check box [ ] and attach sheet with same information and signature and date for each.